FIG.1

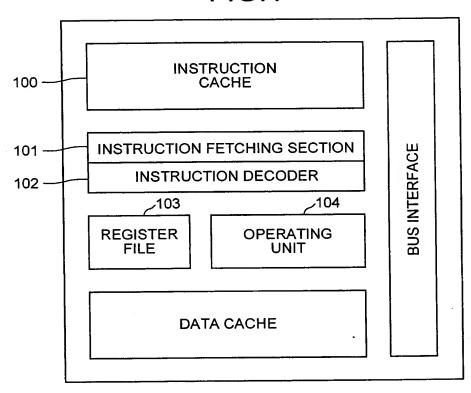


FIG.2

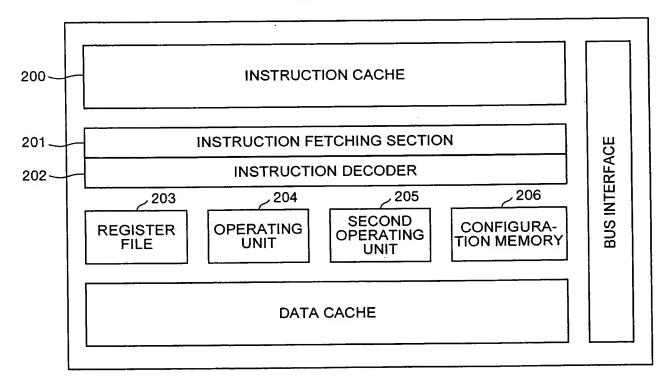


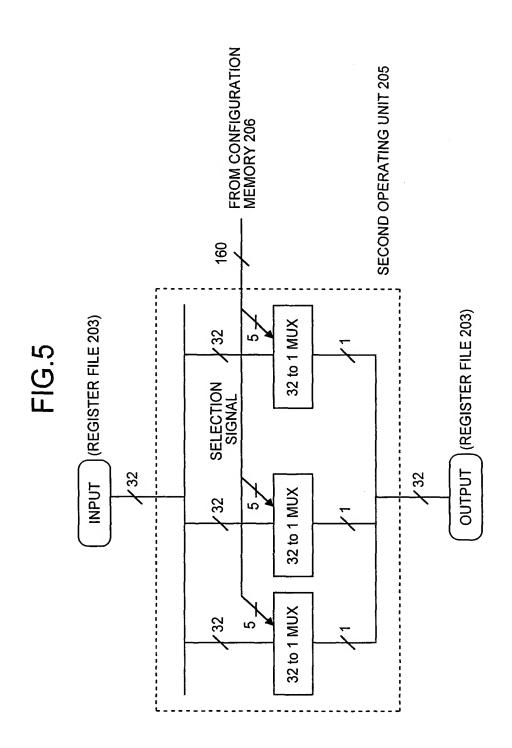
FIG.3

STRUCTURE INFORMATION OF FIRST CUSTOM INSTRUCTION
STRUCTURE INFORMATION OF SECOND CUSTOM INSTRUCTION
STRUCTURE INFORMATION OF THIRD CUSTOM INSTRUCTION
•
•
•
•
STRUCTURE INFORMATION OF
n-TH CUSTOM INSTRUCTION

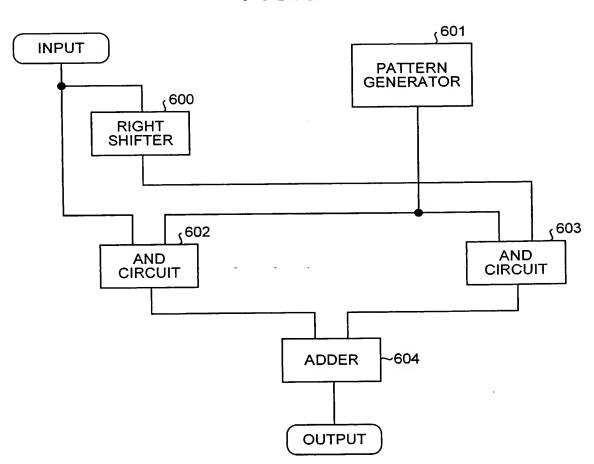
FIG.4

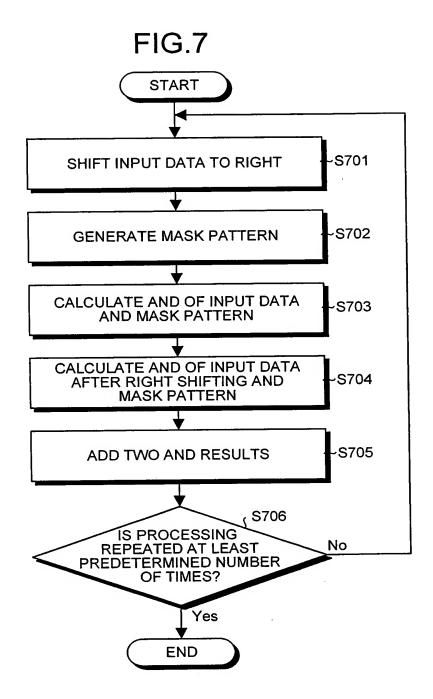
OPERATION CODE THAT SHOWS MEMORY CUSTOM ADDRESS INSTRUCTION	rs1	rs2	rd
---	-----	-----	----

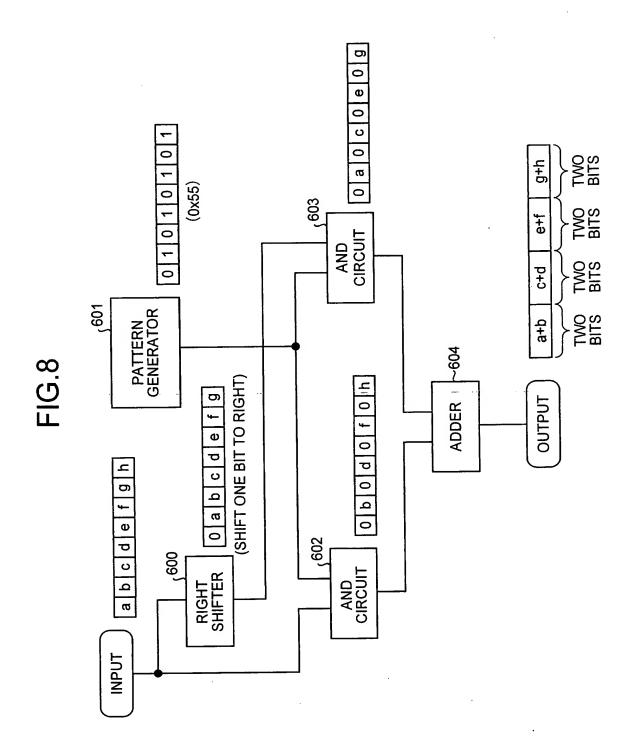
rs1:SOURCE REGISTER 1 rs2:SOURCE REGISTER 2 rd:DESTINATION REGISTER

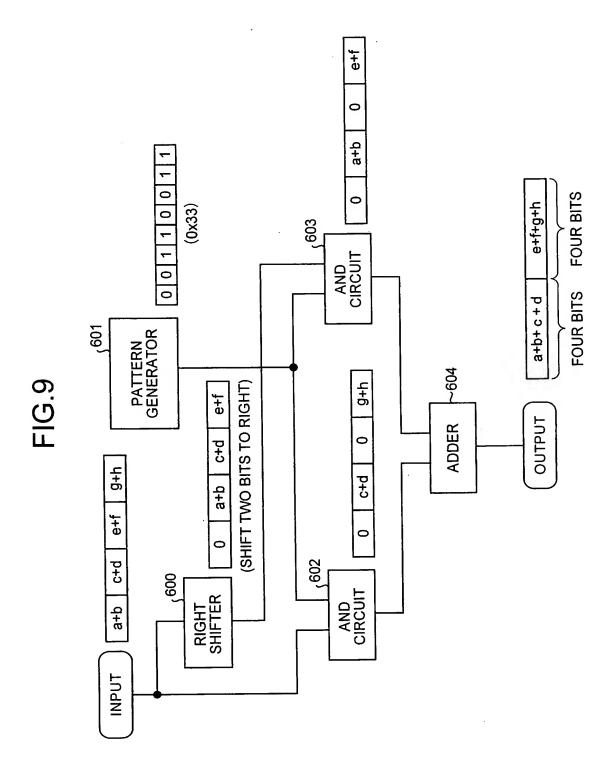












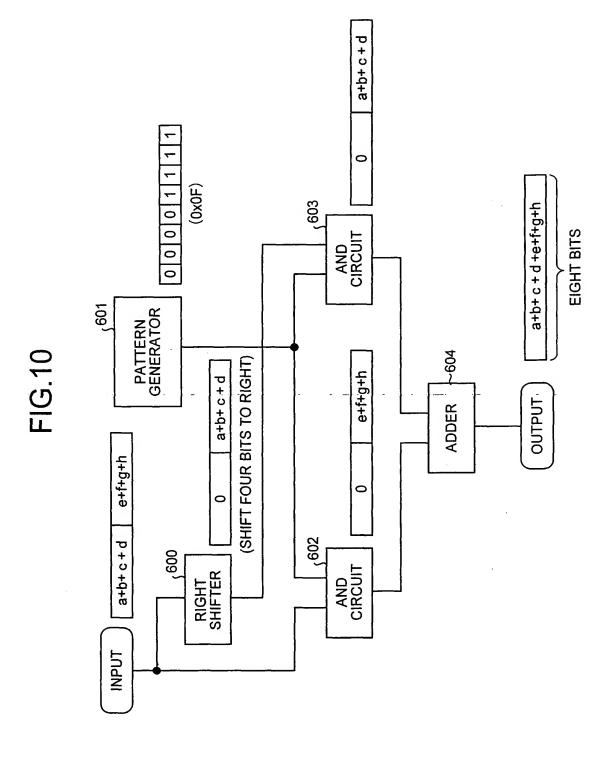


FIG. 11

32 BITS		01010101 01010101 01010101 01010101 (0x5555555)	2	00110011 00110011 00110011 00110011 (0x3333333)	4	00001111 00001111 00001111 00001111 (0x0F0F0F)	8	00000000 1111111 00000000 1111111 (0x00FF00FF)	16	00000000 00000000 1111111 1111111 (0x0000FFFF)
8 BITS	_	01010101(0x55)	7	00110011(0x33)	4	00001111(0x0F)				
	SHIFT QUANTITY	MASK PATTERN	SHIFT	MASK PATTERN	SHIFT	MASK PATTERN		MASK PATTERN	SHIFT QUANTITY	MASK PATTERN
	FIRST	TIME	SECOND	TIME		TIME	FOURTH	TIME	FIFTH	TIME

FIG.12

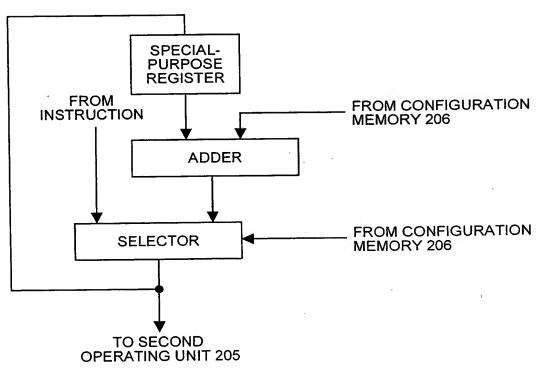
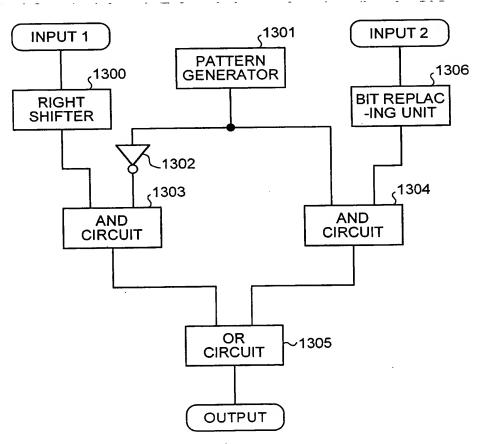


FIG.13



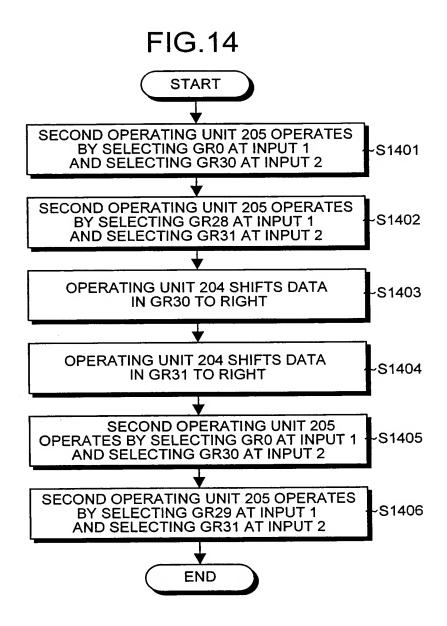


FIG.15

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

FIG.16

58	50	42	34	26	18	10	2
60	52	44	36	28	20	12	4
62	54	46	38	30	22	14	6
64	56	48	40	32	24	16	8
57	49	41	33	25	17	9	1
59	51	43	35	27	19	11	3
61	53	45	37	29	21	13	5
63	55	47	39	31	23	15	7

FIG 17A

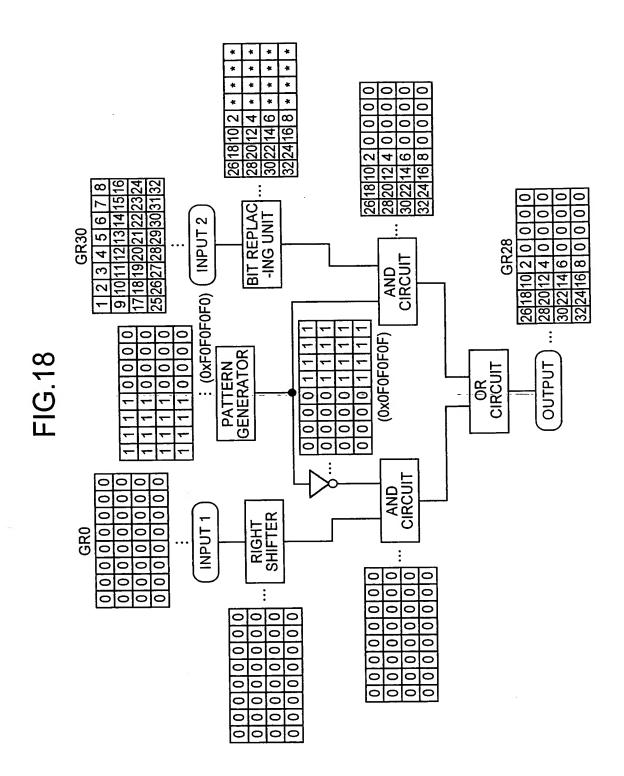
BEFORE REPLACING BITS

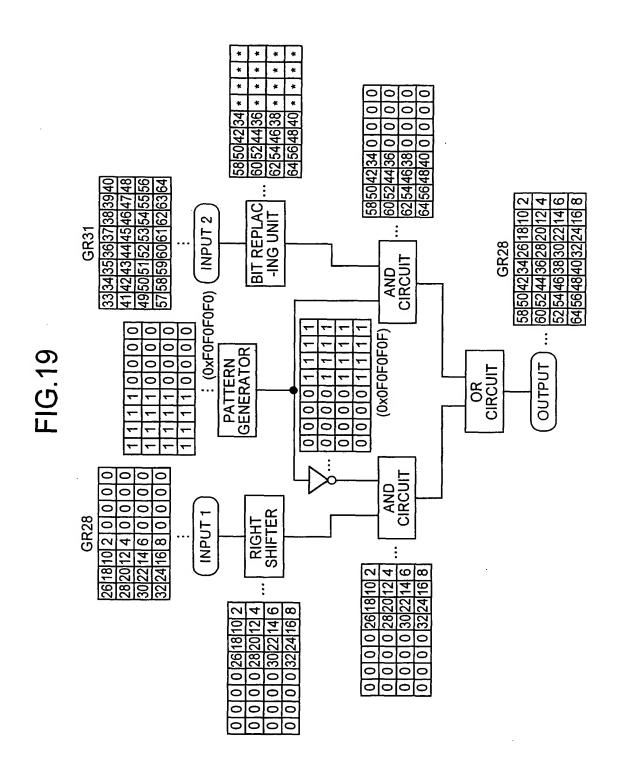
9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 9

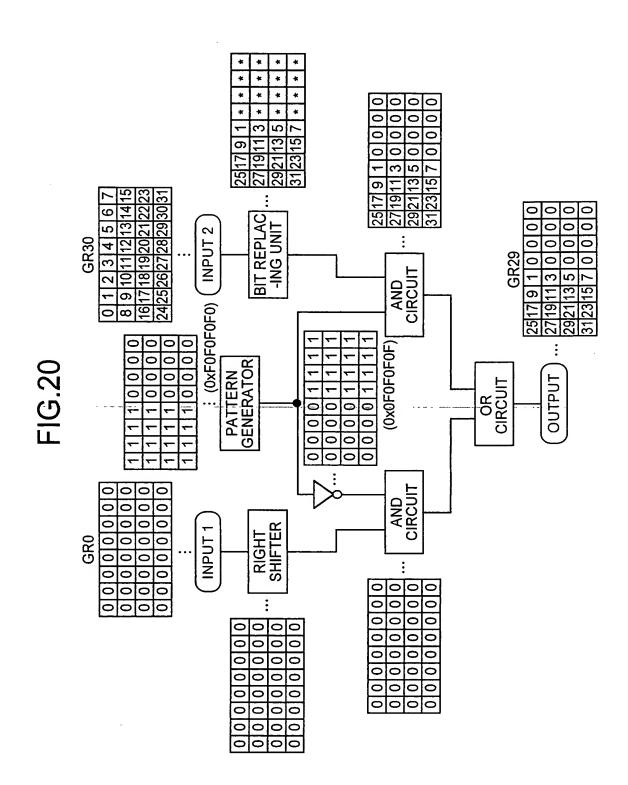
FIG.17B

AFTER REPLACING BITS

* * œ * * * 9 * 30 22 14 * * * 28 20 12 * * 26 18 10 2







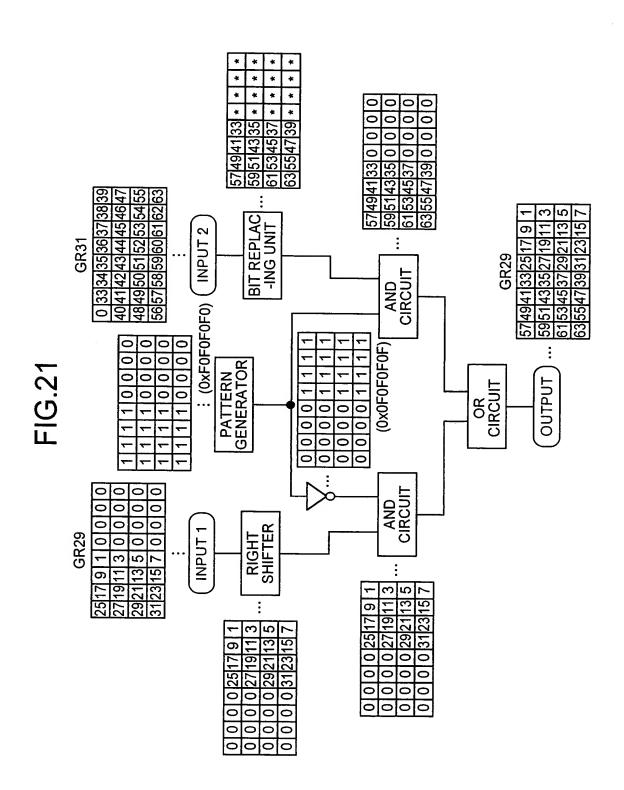
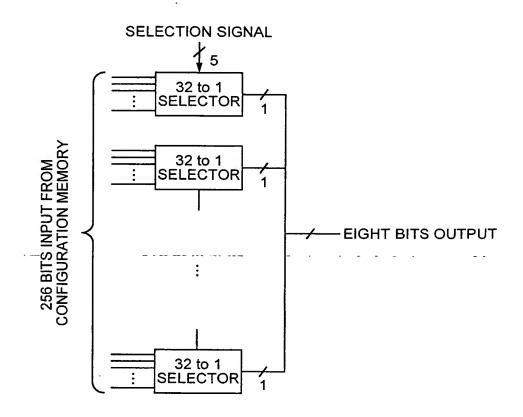


FIG.22



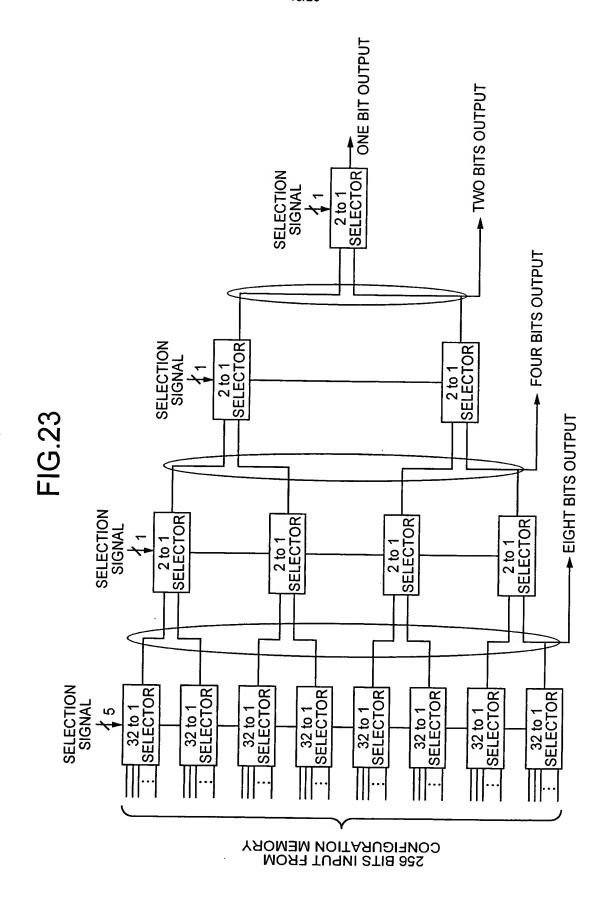


FIG.24

